ZHILICON

Mission-Specific Semiconductors

RISC-V-based semiconductor architectures with workload-specific engines for scientific, secure and mission computing.

Project Brief

ZHILICON develops a common RISC-V architecture with different execution engines for cryptography, molecular research, RF systems, resilient control and artificial intelligence. Each direction is shaped by its workload and integration constraints.

Proposed System Architecture

Workload & Accelerators

A defined mission determines which specialised compute functions the design needs.

Control & Memory

A shared foundation coordinates accelerators and trusted system functions.

Software & Verification

The planned toolchain and design verification must connect the architecture to its intended workload.

Development Requirements

- Workload definition and design verification
- Fabrication and packaging access
- Third-party intellectual property and qualification

What Needs to Be Established

- Which workload and operating requirements justify a mission-specific architecture?
- What performance and energy advantage can be established against available alternatives?
- How do fabrication, packaging and verification requirements affect feasibility and cost?

Customer & Economics

A specialised design needs sufficient demand to justify development and manufacturing costs. Qualification, foundry access, third-party IP and the customer's integration requirements are part of that calculation.

Research & Further Discussion

Research source: RAM LABS

https://ramlabs.xyz/zhilicon.html

For a founder, research, industry or capital discussion, name the venture and the contribution or mandate you bring.

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Prepared 4 November 2026 from the public project description. The system view is conceptual; it does not establish demonstrated performance, incorporation or investment availability.